Implementation of Industrial Narrow Band Communication System into SDR Concept

Marek BOBULA[1], *Karel DANĚK*[2] , *Aleš PROKEŠ*[1]

[1] Dept. of Radio Electronics, Brno University of Technology, Purkyňova 118, 612 00 Brno, Czech Republic
[2] Racom Ltd, Mírova 1283, 592 31 Nové Město na Moravě, Czech Republic

xbobul00@stud.feec.vutbr.cz, karel.danek@racom.eu, prokes@feec.vutbr.cz

Abstract. *The rapid expansion of the digital signal processing has penetrated recently into a sphere of high performance industrial narrow band communication systems which had been for long years dominated by the traditional analog circuit design. Although it brings new potential to even increase the efficiency of the radio channel usage it also forces new challenges and compromises radio designers have to face. In this article we describe the design of the IF sampling industrial narrowband radio receiver, optimize a digital receiver structure implemented in a single FPGA circuit and study the performance of such radio receiver architecture. As an evaluation criterion the communication efficiency in form of maximum usable receiver sensitivity, co-channel rejection, adjacent channel selectivity and radio blocking measurement have been selected.*

Keywords

Radio receivers, radio telemetry, communication system performance, digital radio, software defined digital radio.

1. Introduction

The industrial narrow band communication systems specified mostly by the European standard EN 300 113 [1] are used in challenging environmental and radio conditions. Such systems call for a dynamic range in the vicinity of 100 dB, strict adjacent channel transmitted power requirements, high data sensitivity, adjacent channel selectivity, radio blocking or desensitization, co-channel rejection and others [1],[2]. It is no wonder that for such high dynamic range demands super heterodyne receiver structure is being widely used. But yet the radio transceiver has to be small in dimensions, consuming low power and remains all the parameters over wide industrial temperature range and over the extensive period of time for reasonable price and at the same time provides enough flexibility to accommodate different channel bandwidths, various digital modulations formats and data rates. From this point of view the SDR (Software Defined Radio) concept is indisputably a prospective alternative.

Although the SDR principles and various algorithms evaluations are favored by an overwhelming interest in technical literature, we feel the gap in discussing the overall system performance when the SDR concept is employed in a narrow band radio transceiver design. The exceptions can be seen in references [2], [3]. In reference [3] the authors deal with a similar task of in-building base station design, however the specific aspects which take place in the design of the narrow band communication system according to [1] differ and are not discussed.

Originated in the previous work and results published in [2] the goal of this article is to achieve an understanding of the limitation and compromises influencing the dynamic range performance of the IF (Intermediate Frequency) sampling digital receiver with a main emphasis on its practical implementation.

The main design objectives of this prototype can thus be described as follows:

- Design an IF sampling digital receiver intended for the narrow band industrial radio transceiver which meets EN 300 113 specification [1] using single chip FPGA SDR approach.
- Optimize the digital signal receiver chain resolution respecting the dynamic range performance and power dissipation of the digital receiver.
- Determine the main limitations of the proposed concept and evaluate the data sensitivity and other essential radio receiver parameters.
- Determine the IF sampling digital receiver requirements upon the preceding analog front-end part in order to fulfill the EN 300 113 specification [1].
- Evaluate the communication efficiency of the overall communication system in form of receiver data sensitivity and radio blocking measurement.

The narrow band industrial communication system specified by [1] uses 25/20 kHz channel spacing, with channel bandwidths of 25/12.5/6.25 kHz. The system uses a constant envelope modulation M–CPFSK with h=1/M at least due to the strict adjacent channel transmitted power requirements and the need for good power and spectral

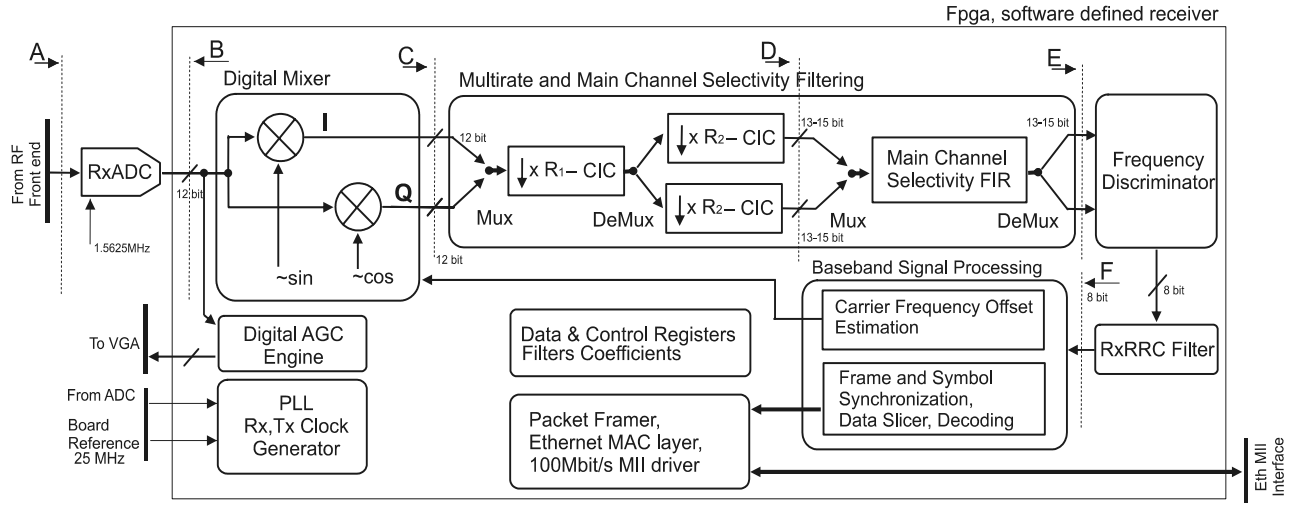

Fig. 1. Proposed IF sampling digital receiver structure implemented in an FPGA circuit. The capitals denote the main design stages where the bit optimization was performed in order to satisfy the design objectives.

efficiency reaching 1 bit/s/Hz. Other parameters related to the design process can be seen in:

- Data sensitivity better that –113 dBm, (25 kHz).
- Adjacent channel selectivity better than 70 dB.
- Radio blocking and desensitization better than 84 dB.
- Receive/transmit switching time less than 1.5 ms.
- Radio reference oscillator stability of ±0.5 ppm.
- RF frequency of operation from 70 MHz up to 1 GHz.

2. Digital Radio System Architecture

We start the design process of the IF sampling digital narrow band receiver shown in Fig.1 by analyzing the ADC (Analog to Digital Converter) parameters which have certainly a crucial impact on its overall dynamic range performance. The maximum bit resolution of the ADC (Fig. 1, B) is driven mainly by two requirements. As shown in [6], one is the minimum SNR_{req} (Signal to Noise Ratio) required for the digital demodulator to process the incoming signal with an acceptable number of errors. The second – and the major aspect here – is the available effective dynamic range of the digital part of the receiver. Its upper limit is determined by the full scale level of the ADC as an alternative to a 1dB compression point of the analog receiver and the lower, by all sources of noise introduced in the quantization process within the frequency band of our interest. It needs to be noted that such definition is not the exact equivalent to its analog counterpart mainly because the distortion products of the ADC do not tend to vary as a function of signal amplitude [2]. With a feasibility of the digital design in mind we can write the effective dynamic range of the ADC stage in form of signal to noise ratio within a specified bandwidth as

$$SNR_{ADC} = 6.02(ENOB) + 1.76 + 10\log\left(\frac{f_s}{2.B_N}\right) \quad (1)$$

where we take an effective number of ADC bits (*ENOB*) [13], rather then nominal number of ADC bits *N* [6],[15]. f_s is a sampling frequency, B_N is a noise bandwidth of 25 kHz unless otherwise noted and their ratio is usually addressed as OSR (Over Sampling Ratio) or processing gain in [dB]. We see that to increase the dynamic range of the ADC we could simply increase the number of effective bits and/or increase the sampling frequency. In a real application we are unfortunately limited in both. As the frequency of the processed IF signal increases (Fig. 2), it is becoming difficult to reach sufficient signal resolution mostly due to the aperture jitter which is a significant ADC dynamic range performance limitation (2) [7].

$$SNR_{jitter\_limited} = -20\log\left(2\pi f_{IF} t_{j,rms}\right)[dB] \quad (2)$$

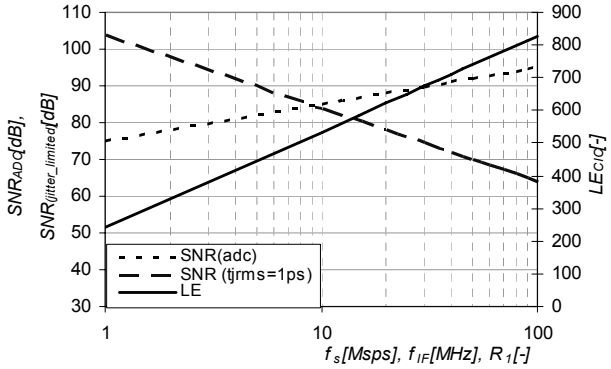

Fig. 2. *(short dashed)* Processing gain influenced SNR_{ADC} (1) of the *ENOB*=10 bits A/D converter over the increasing sampling frequency. *(long dashed)* The tendency of the jitter limited SNR versus input IF frequency (aperture jitter assumed t_{jrms}=1 ps) (2),[7]. *(solid)* An example of the trade-off between the decimation CIC filter FPGA logic elements count versus an increase in sampling frequency and decimation ratio R_1.

On the other hand as the sampling frequency increases, the requirements upon the follow-up digital down conversion and demodulation stage ramp–up significantly. As an example a typical increase in LE (Logic Elements [14]) count of the digital CIC (Cascaded Integrator Comb) filter FPGA implementation versus an increasing decimation ratio R_1 is shown in Fig. 2. In addition, both operations are directly related with a negative tendency in power consumption. Moreover, we have to consider the practical aspects of the analog front-end design where the placement of the first IF is typically at frequencies ranging from 40 MHz to 75 MHz depending for instance on an availability of the SAW or crystal filters. By concerning all these aspects we have chosen to sub-sample the first intermediate frequency of 45 MHz with a relatively low sampling frequency in the vicinity of 1 MHz (1.5625 MHz). The situation is depicted in Fig. 3 from which we can estimate the effective input signal resolution. By using equations (1) and (3) [15]:

$$SNR_{ADC} = d - 10\log\left(\frac{N_{FFT}}{2}\right)[dB] \tag{3}$$

where d is a difference between the input signal level and the average value of noise power spectrum density and N_{FFT} is a length of the Fast Fourier Transform used to calculate the spectrogram – we can find the actual $ENOB \approx 13$ bits which is the starting point in the IF digital receiver design bit optimization.

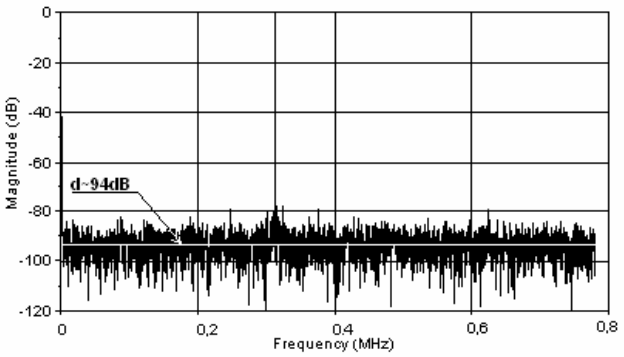

Fig. 3. Normalized 8k FFT spectrum plot of the sub–sampled IF signal with an input level of –1 dBFS of the 12-bit A/D converter. We can estimate the $SDR_{ADC} \approx 58$ dB (3) or 76 dB including the processing gain shown in (1).

Note that this value includes the processing gain (1) which however, does not take place before the filtering stage (Fig. 1 D,E). Thus at the B stage (Fig. 1) the input signal has lower effective resolution available of approximately 10 bits ($SNR_{ADC} \approx 58$ dB) in relation to the whole 1st Nyquist's zone. This is a key fact for selecting the DDC (Digital Down Conversion) stage comprising the complex NCO (Numerically Controlled Oscillator) and embedded multipliers. Since this part runs at the highest clock of the whole digital receiver it makes sense to design it carefully. To realize how the bit resolution of the NCO influences the effective dynamic range of the digital receiver we set up a simulation to measure the noise power spectral density at the output of the digital down conversion stage (Fig. 1 B, C). The input signal ENOB was assigned to 10 bits which sets the reference level (0 dB) for the normalized noise PSD as it is shown in Fig. 4. The ideal floating point realization of the DDC in this case would yield to –3dB level in each signal path. As can also be seen in Fig. 4, it is sufficient to choose the NCO resolution with 2 bits exceeding the effective input signal resolution without a significant degradation of the effective dynamic range in the digital mixing stage. On the other hand choosing a higher resolution of the NCO and down converted signals would not bring any advantage and would cause an increase in logic elements count and power consumption. Please note that the NCO assumed in this example is generating an output frequency not having a fundamental relation to the sampling frequency such as *fs*/4. In this special case the signal resolution is optimal, even though the NCO is generating only <0, 1, 0, -1> values.

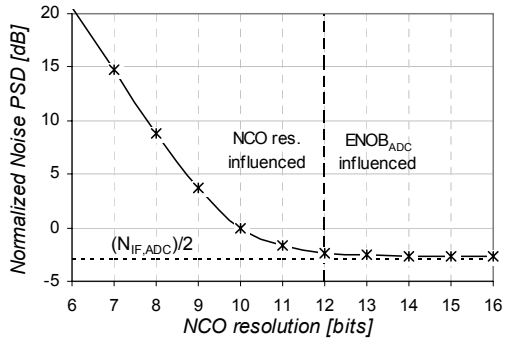

Fig. 4. Normalized noise power spectral density increase in InPhase (Quadrature) signal path after digital mixing (Fig.1,C) as a function of complex NCO signal bit resolution.

One of the main advantages of the digital receiver architecture can be seen in a use of precise digital filters of all types. Their usage in the practical narrow band digital receiver is at up most importance; however, it is followed by two main limitations. First – and the minor one – is a general ramp-up in an implementation complexity with increasing over-sample ratio previously mentioned in relation to (1). This problem can be partially reduced by the combination of the CIC filters preceding the FIR (Finite Impulse Response) filter stages, mainly due to their effective realization structures requiring no multipliers or coefficient storage. Further optimization can be done by multiplexing the I and Q signal paths together and using one filter structure as shown in Fig. 1 or using other wise "DSP tricks" e.g. [8]. In any case the digital filters consume a significant part of the FPGA resources especially if the high demanding fully parallel structures are needed [9].

The second aspect of the digital filters utilization in narrow band digital receiver architecture is a fact that their selectivity and filtering ability does not help to prevent ADC saturation and some kind of AGC (Automatic Gain Control) algorithm is required to be employed in the system prior to the filtering stage (Fig. 1). Thus for high level

interfering signals the digital filtering is helpless, even though we design a filter with the highest stop band attenuation available. Placing the AGC block after the main channel selectivity filters would also not easy the problem and the AGC response would need to accommodate the whole impulse response of the preceding signal path to maintain stability. Naturally, this fact forces a tighter requirements upon the preceding analog filter, which not only needs to provide an anti-aliasing band limitation necessary for the sub-sampling technique, but it also needs to undertake a portion of the main channel selectivity as will be shown by the results of the digital receiver system simulations.

The digital filtering is exactly the stage where the processing gain (1) takes place as shown in Fig. 5. Thus depending on a channel bandwidth selected the signal resolution in D and E stages (Fig. 1) should have ENOB of 13 to 15 bits for the processing gain to take its effect. This is a natural fact which is hidden in equation (1) and is sometimes not perceived properly in the digital receiver design. In an imaginary situation, where the digital filter input signal is corrupted by the lowest quantization noise of its least significant bit only, the filter with an input and output bit width, which is equivalent to the signal resolution, cannot help to suppress the quantization noise further. In a real situation however, where the noise caused by the quantization process is always little bit higher it would partially take its effect, but the correct way to accommodate the processing gain is to adequately increase the filter resolution.

The proposed filtering part of the design is based on four stage multiplexed CIC filter [8] with the decimation factor R_1=15. It is followed by the two stage CIC filters with the decimation factor of R_2=1, 2, 4. Main channel selectivity filter is designed as 42 tap FIR filter having a fully serial filter structure [9] and a -3 dB low pass bandwidth of 0.75**SymbolRate.* All amplitude frequency characteristics are shown in Fig. 5.

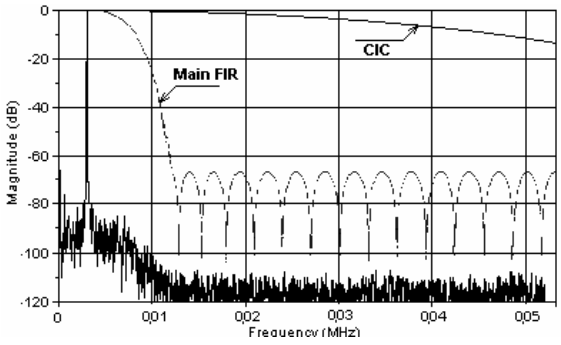

Fig. 5. 8k FFT spectrum plot of the InPhase signal after the decimation and main channel filtering stage (Fig. 1, E). The processing gain introduced by the digital filtering (1) is available only after appropriate output bit resolution adjustment.

There is a number of ways how to implement a digital frequency demodulator [10], [11]. In this project we used a digital approach based on a discrete time signal differentiation as an approximation to the modulated signal phase derivation [12]:

$$m[n] = \frac{\left(x_I[n-1]x_Q[n] - x_I[n]x_Q[n-1]\right)}{(\pi h / N)\left[(x_I[n])^2 + (x_Q[n])^2\right]}. \quad (4)$$

Here the $m[n]$ can be seen as a reconstructed replica of the transmitted modulation signal, N is the number of samples per symbol, h is a modulation index of the M–CPFSK modulation, x_I and x_Q (Fig. 1, E) are the complex baseband signal samples taken in a time instant $n.T_s$ [12]. Respecting the constant magnitude character of the M–CPFSK modulated signal we can see that the whole denominator of equation (4) is a constant. Although it is definitely true for the transmitted signal – if no additional channel filtering is performed by the transmitter – the received signal has a significant magnitude variance caused mostly by the main channel selectivity filter. This amplitude variance cannot be omitted in a digital CPFSK baseband receiver and the denominator should be implemented in the system. It can also be seen as a digital signal normalizer and it is the last block with a direct impact on a dynamic range performance of the proposed digital receiver. It therefore consumes a significant part of the FPGA logic resources.

The following stages, particularly the RxRRC (Root Raised Cosine) filtering, symbol synchronization, carrier frequency offset compensation and data receiver work with a normalized input signal and as such they are not closely covered within the scope of this article. However, they create a significant part of the design process and they have been implemented in a proposed reconfigurable digital narrow band receiver [12].

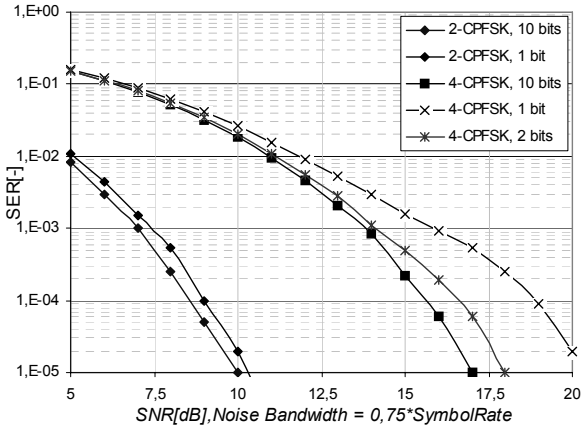

Fig. 6. Power efficiency characteristics for 4–CPFSK and 2–CPFSK digital narrow band receiver for 1 and 10 bits effective input signal resolutions. The results are based on a bit stream simulation over more than 10^5 symbols.

3. Simulation Results

We set up a simulation to analyze the proposed structure of the digital receiver using ALTERA's DSPbuilder toolbox for MATLAB Simulink software. We

were focused on two utmost situations, which have been derived in previous section. In first, the resolution of the input signal has been set to the value equivalent to a full-scale level of the 12 bit ADC with *ENOB*=10 bits (Fig. 3). In second, the input signal level has been set to have an effective resolution of 1 bit above the two least significant "noisy" bits of the ADC. In both cases the increased level of ADC noise floor has been simulated by independent noise generator having the signal resolution of two bits which were added to the input signal. Other parameters of the simulation are as follows:

- 4–CPFSK and 2–CPFSK modulations with the modulation indexes h=0.25, h=0.75 respectively.
- Symbol rate of R=10.417 ksymbols/s.
- TxRRC and RxRRC filters with *roll–off*=0.28.
- 25 kHz band limited AWGN noise generator with real power spectrum density N_0.

Fig. 6 illustrates the SER (Symbol Error Rate) performance of the proposed receiver structure over an increasing input signal SNR ratio. It can readily be seen that for 2–CPFSK modulation the input signal SNR in combination with the processing gain is sufficient for the correct operation and there is almost no degradation in power efficiency even with the 1 bit of effective input signal resolution. On the other hand, for 4–CPFSK modulation the combination of the input and simulated ADC noise levels falls to the area of our interest where $SER=10^{-5}$ and causes a significant degradation in power efficiency. It needs to be noted that the result is also influenced by a finite resolution of the differentiation process, which we suppose is becoming evident with a lower signal resolution.

By using the results of the previous simulation and a full scale level of the ADC – in our case approximately -6 dBm (50 Ω) – one can easily evaluate the data sensitivity of the proposed IF sampling digital part of the narrow band receiver.

We set up a second simulation to analyze the co-channel rejection, adjacent channel selectivity, radio blocking and desensitization parameters according to [1]. These parameters in general, are the measures of the capability of the receiver to receive a weak wanted modulated signal without exceeding a given degradation due to the presence of an unwanted signal. Measuring methods used for evaluating of these parameters differ in unwanted signal frequency, which equals to the nominal receiver frequency; differs from the nominal receiver frequency by an amount of the adjacent channel separation; or is of any frequency other than the frequencies of the spurious responses and the adjacent channels. There are also different – very strict, but reasonable – limits required for each parameter that should not be less than:

- -8 dB to 0 dB for co-channel rejection
- 70 dB for adjacent channel selectivity
- 84 dB for radio blocking ratio

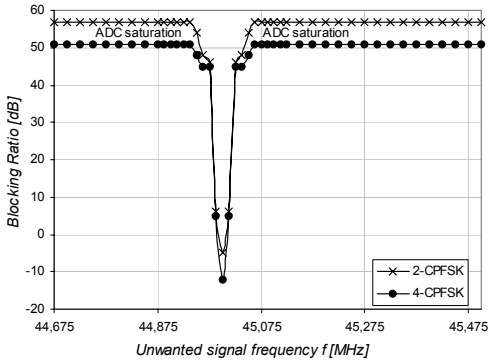

Fig. 7. The result of the co-channel rejection, adjacent channel selectivity, radio blocking and desensitization simulations for the frequency band of one Nyquist's zone of 0,78125 MHz around the IF frequency of 45 MHz.

As can be seen in Fig.7 only the IF sampling digital receiver itself cannot and does not fulfill such strict requirements, mainly because of the limited dynamic range of the ADC. The widening of the processed Nyquist's zone and thus increasing the dynamic range by additional processing gain (1) might be an option here, but the trade off will be paid in complexity – hence power consumption and price – of the digital down converter and demodulation stage. We are convinced however, that the analog front-end design in a wise combination of the digital receiver based on today's technology is still essential to improve the sensitivity, adjacent channel selectivity and to extend the dynamic range of the whole narrow band receiver.

4. Analog Front-End and Digital Receiver Signal Resolution

To satisfy the design objectives and not to degrade the performance of the 4–CPFSK modulation by the ADC noise for more than 1 dB at $SER=10^{-5}$ the preceding analog front-end part should provide enough gain for the thermal noise coming from the input low noise amplifier to become dominant over the ADC noise level.

Firstly, we need to calculate the worst case noise figure *NF* [6] of the analog front-end part with regards to the demanded maximum usable sensitivity of the receiver as:

$$NF = S - 10.\log(k.T) - 10.\log(B_N) - SNR_{req} \quad (5)$$

where S is a maximum usable sensitivity signal level (our particular calculation is made for the case of the standard [1] fulfillment, in which maximum usable sensitivity shall not exceed an emf (electromotive force) +3 dBμV). B_N is a noise bandwidth and SNR_{req} is a signal to noise ratio acquired from the system simulations (Fig. 6), for the specified BER level of the least power efficient modulation technique in the system. As defined in [1] the BER value shall not exceed 10^{-2} for the presented maximum usable sensitivity signal level. Then, an example of the NF calculation using the design objectives can be written as:

$$NF = -110\text{dBm} + 174\text{dBm/Hz} - 44\text{dBHz} - 11\text{dB}_{4\text{CPFSK,10e-2}}$$
$$NF = 9\,\text{dB}. \quad (6)$$

As a second, we can calculate the overall analog front gain G_{FE} as follows:

$$G_{FE} = \{ADC_{FS} - EDR\} - \left\{10.\log(k.T) + NF + 10.\log\left(\frac{f_s}{2}\right)\right\}. \quad (7)$$

Here the ADC_{FS} represents the full scale level of the ADC, EDR is the effective dynamic range of the digital receiver found by the system simulation, k is Boltzmann constant and T is the absolute temperature in Kelvins. In (7) the effective dynamic range EDR describes the ability of the digital receiver to process the incoming digital signal. We see that the wider the EDR the less front-end gain is required and the better values of selectivity and blocking can be reached only by the digital part of the receiver. The value of EDR should already include a reasonable gain margin to suppress the noise contributions of a real ADC device. In our particular example we can write:

$$G_{FE} = \{-6\,\text{dBm} - 50\,\text{dB}\} - \{-174\,\text{dBm/Hz} + 9\,\text{dB} + 59\,\text{dBHz}\}$$
$$G_{FE} = 50\,\text{dB}. \quad (8)$$

The calculated analog front-end gain required for the proper function of the software defined digital radio receiver with selected parameters is rather high which is caused mainly by an extensive equivalent noise figure of the ADC. The noise figure and gain values of the analog front-end can be calculated in other ways indeed, but the two step calculation being described is very effective in developmental practice, in which the compliance requirements that meet the demand for the high dynamic range is of the most importance. In such a case, the acquired values of the analog front-end noise figure and gain should be taken into account and we should add only a small margin to them, with a necessary amount of serendipity. Thirdly, a suitable anti-aliasing filter has to be chosen. We can see from Fig. 7 that notwithstanding the fact, that the digital filters bear the major part of the channel selectivity, the use of the anti-aliasing filter with a steep bandpass response – typical for crystal filters and SAW (Surface Acoustic Wave) devices – is preferable characteristic for the proposed analog front-end system. Care must be taken in this case to the typical "analog world" parameters such as proper impedance matching; group delay response etc.; otherwise impairment of the radio channel linearity is introduced and troublesome to compensate.

5. Measurement Results and Conclusion

We adopted the design procedure described in the previous sections for the prototype narrow band radio construction based on FPGA circuit and carried out initial measurements.

Fig. 8 depicts the results of the maximum usable sensitivity measurement for the complete radio receiver. We see that the emf limit of +3 dBμV (-110 dBm, 50 Ω) demanded by [1] is fulfilled with a small margin even for the 4–CPFSK modulation.

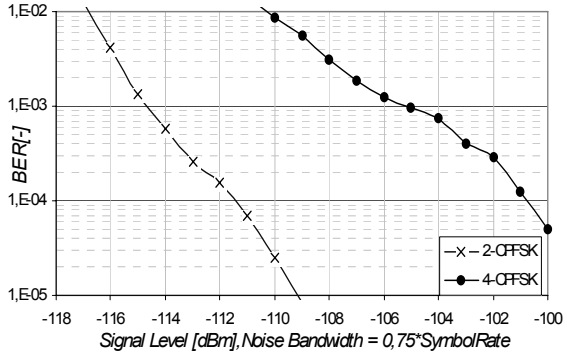

Fig. 8. The result of the maximum usable sensitivity measurement of the narrow band receiver for 25 kHz channel bandwidth.

It needs to be noted however, that the actual values of BER have been calculated from the packet error rates PER according to (9) where N_{bytes} is the number of bytes in a received packet. Thus they might be encumbered with a small inaccuracy.

$$BER = 1 - (1 - PER)^{\frac{1}{8.N_{bytes}}} \quad (9)$$

Although the results are influenced by synchronization, carrier signal level and frequency offset errors, they reflect the complete radio system performance well.

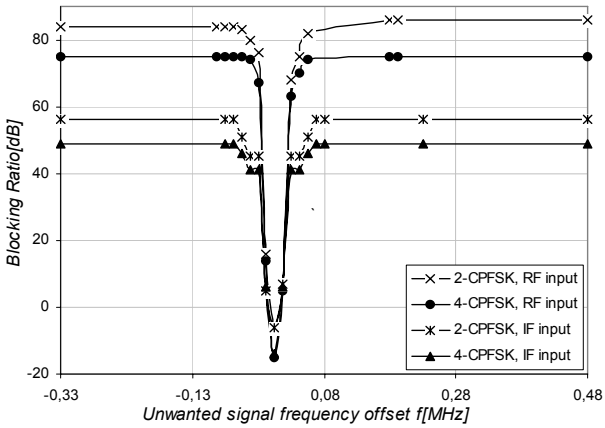

Fig. 9. The result of the co-channel rejection, adjacent channel selectivity, radio blocking and desensitization measurements for the frequency band of one Nyquist's zone of 0.78125 MHz around the RF frequency of 409.025 MHz and around the IF frequency of 45 MHz.

As a second, the essential radio parameters for the IF sampling digital receiver as well as for the complete radio solution have been measured and the results are shown in Fig. 9. It can be seen from it that the results for the software defined digital part differ from the simulated ones

(Fig. 7) for less than 3 dB which can be judged acceptable for the practical realization. Moreover we can see that the requirements of the standard [1] are met fully for 2–CPFSK mode of operation. For 4–CPFSK modulation there is still need for further optimization especially in radio blocking parameter which will be the main scope of the future work.

The IF sampling software defined digital radio intended for narrow band industrial applications was implemented in a single Altera's Cyclone II EP2C8T144I8 FPGA device [14]. Together with the transmitter part, proprietary Ethernet MAC, radio controllers etc., the complete solution consumes 80% of LEs, 35% of memory bits, 60% of embedded multipliers and drives approximately 80 mW of power, while running at 25 MHz system clock.

As we tried to show in this article, when designing the high demanding digital applications such as modern wide dynamic range software defined radio the right and in all conscience inconsiderable portion of analog front-end circuitry is still needed and such compromised mixed signal solution better avails the powerful potential of today's digital signal processing circuits available and suitable for the application.

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About Authors...

Marek BOBULA was born in 1983 in Svit, Slovakia. He graduated at the Brno University of Technology in 2006 and received MSc degree. Since 2006 he is engaged in research and development in the field of digital radio signal processing in Racom Ltd. with a main emphasis on FPGA technology. He is currently a postgraduate student at the Department of Radio Electronics, BUT.

Karel DANĚK was born in Nové Město na Moravě, Czech Republic, in 1961. He received his MSc and PhD degrees from the Brno University of Technology, Department of Telecommunication in 1984 and 2001, respectively. He is author of a number of articles and a book *"Moderní rádiový přijímač, Kniha o jeho návrhu",* published in Prague, 2005. Since 1991 he is a chief hardware designer in Racom Company. His present professional interests are in the land mobile radio communications, RF and software digital radio circuit design.

Aleš PROKEŠ was born in Znojmo, Czech Republic, in 1963. He received the MSc and PhD degrees in Electrical Engineering from the Brno University of Technology, Czech Republic, in 1988 and 2000, respectively. He is currently an Assistant Professor at the Brno University of Technology, Department of Radio Electronics. His research interests include nonuniform sampling, velocity measurement based on spatial filtering and free-space optical communication with emphasis on optical receiver performance analysis and optimization.